AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-37. (Canceled)

38. (Currently Amended) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming an interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the interfacial layer, the high dielectric constant layer comprising $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, and wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer;

(d) forming source and drain regions in the substrate adjacent to the gate electrode; and

(e) forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer by depositing a film selected from the group consisting of

phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film; and

(f) forming second spacers on an upper surface of the interfacial layer adjacent to the spacers formed in step (e) and to the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film.

39. (Previously Presented) The method of Claim 38 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

40. (Previously Presented) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming an interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the interfacial layer, the high dielectric constant layer comprising a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, and wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer; and

(d) forming source and drain regions in the substrate adjacent to the gate electrode.

41. (Previously Presented) The method of Claim 40 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

42. (Previously Presented) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming an interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the interfacial layer, the high dielectric constant layer comprising a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer; and

(d) forming source and drain regions in the substrate adjacent to the gate electrode.

43. (Previously Presented) The method of Claim 42 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

44. (Currently Amended) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming a silicon nitride interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the silicon nitride interfacial layer, the high dielectric constant layer comprising a material that is selected from the group consisting of Ta_2O_5, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, and mixtures thereof wherein the silicon nitride interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer;

(d) forming source and drain regions in the substrate adjacent to the gate electrode; and

(e) forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film; and

(f) forming second spacers on an upper surface of the interfacial layer adjacent to the spacers formed in step (e) and to the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film.

45. (Currently Amended) A method for fabricating a MOS device having a gate width of less than 0.3 micron, comprising:

(a) forming an interfacial layer on a semiconductor substrate;

(b) forming a high dielectric constant layer on the interfacial layer, the high dielectric constant layer comprising a material selected from the group consisting of

$Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6,

a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, and

a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1,

wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) forming a gate electrode of an electrically conductive material on the high dielectric constant layer;

(d) forming source and drain regions in the substrate adjacent to the gate electrode; and

(e) forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film; and

(f) forming second spacers on an upper surface of the interfacial layer adjacent to the spacers formed in step (e) and to the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film.

46. (Previously Presented) The method of Claim 38 wherein the interfacial layer comprises silicon oxide.

47. (Previously Presented) The method of Claim 38 wherein the interfacial layer comprises silicon nitride or silicon oxynitride.

48. (Canceled)

49. (Previously Presented) The method of Claim 45 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

50. (Previously Presented) The method of Claim 38 wherein the interfacial layer and the high dielectric constant layer separates the spacers from the substrate.

51. (Previously Presented) The method of Claim 44 wherein the interfacial layer and the high dielectric constant layer separates the spacers from the substrate.

52. (Previously Presented) The method of Claim 45 wherein the interfacial layer and the high dielectric constant layer separates the spacers from the substrate.

53. (Canceled)

54. (Canceled)

55. (Canceled)